Notice of Allowability	Application No.	Applicant(s)	
	09/823,085	CONG ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *25 May 2005*.

2. ☒ The allowed claim(s) is/are *1,4-8,10-12,15-19,21 and 22*.

3. ☒ The drawings filed on *01 October 2004* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/17/01 & 10/20/02
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicant's communication dated May 24, 2005. Claims 4 and 15 were amended. Claims 1-33 of the application are pending.

Drawings

2. The drawings submitted on October 1, 2004 are accepted.

Examiner's Amendment

3. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Michael Mallie on July 29, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

4. In Claim 1:

Replace claim 1 with:

1. A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determining a coupling between the victim net and the aggressor;

determining noise width using the model of the victim;

determining peak noise amplitude using the model of the victim net; and

indicating that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 2:

Delete Claim 2.

In Claim 3:

Delete Claim 3.

In Claim 6:

Replace claim 6 with:

6. A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determining a coupling between the victim net and the aggressor;

determining noise width, wherein the noise width is determined corresponding to:

$t_r + t_v \ln[(1- e^{-2t_r/t_v})/ (1- e^{-t_r/t_v})]$

where t_r comprises transition time and t_v comprises a distributed Elmore delay of the victim net;

determining peak noise amplitude using the model of the victim net; and

indicating that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 7:

Replace claim 7 with:

7. A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determining a coupling between the victim net and the aggressor;

determining noise width, wherein the noise width is based on only transition time and distributed Elmore delay of the victim net;

determining peak noise amplitude using the model of the victim net; and

indicating that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 8:

Replace claim 8 with:

8. A method for identifying potential noise failures in an integrated circuit design comprising:

locating a victim net and an aggressor within the integrated circuit design;

modeling the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determining a coupling between the victim net and the aggressor;

determining noise width, wherein the noise width is independent of an RC delay term from upstream resistance of the coupling element times coupling capacitance of the coupling location;

determining peak noise amplitude using the model of the victim net; and

indicating that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 9:

Delete Claim 9.

In Claim 12:

Replace claim 12 with:

12. An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determine a coupling between the victim net and the aggressor;

determine noise width using the model of the victim;

determine peak noise amplitude using the model of the victim net; and

indicate that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 13:

Delete Claim 13.

In Claim 14:

Delete Claim 14.

In Claim 17:

Replace claim 17 with:

17. An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determine a coupling between the victim net and the aggressor;

determine noise width, wherein the noise width is determined corresponding to:

$t_r + t_v \ln[(1- e^{-2t / t_r t_v})/ (1- e^{-t / t_r t_v})]$

where t_r comprises transition time and t_v comprises a distributed Elmore delay of the victim net;

determine peak noise amplitude using the model of the victim net; and

indicate that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 18:

Replace claim 18 with:

18. An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determine a coupling between the victim net and the aggressor;

determine noise width, wherein the noise width is based on only transition time and distributed Elmore delay of the victim net;

determine peak noise amplitude using the model of the victim net; and

indicate that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 19:

Replace claim 19 with:

19. An article of manufacture comprising one or more recordable medium having executable instructions stored thereon which, when executed by a system, cause the system to:

locate a victim net and an aggressor within the integrated circuit design;

model the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location;

determine a coupling between the victim net and the aggressor;

determine noise width, wherein the noise width is independent of an RC delay term from upstream resistance of the coupling element times coupling capacitance of the coupling location;

determine peak noise amplitude using the model of the victim net; and

indicate that the integrated circuit design requires modification if the noise width or the peak noise amplitude indicates that a potential noise failure will occur in the integrated circuit design.

In Claim 20:

Delete Claim 20.

In Claims 23-33:

Delete Claims 23-33.

A clean copy of the amended claims is attached.

Reasons for Allowance

5. Claims 1, 4-8, 10-12, 15-19, 21 and 22 of the application are allowed over prior art of record.

6. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) an automated method of analyzing crosstalk in an integrated circuit; for at least one potential victim wire, subset of potential aggressor wires that may couple to the victim wire are found; the aggressor wires are combined into a common aggressor; a rise time of the common aggressor is calculated and used to calculate the magnitude of the coupled noise on the victim wire induced by the aggressor wires; an alarm threshold for each potential victim wire is determined based on the type of the logic gate that receives the victim wire; the alarm threshold for each potential victim wire is compared to the calculated coupled noise of the victim wire to determine if any wires of the design suffer enough crosstalk noise that they should be redesigned (**Aingaran et al.,** U. S. Patent 6,536,022);

(2) improved analytical models for interconnect coupling noise due to coupling capacitance; applying the Phi model to the segmented aggressor case; a linear driver resistance is included in the modeling of both the victims and the aggressors to measure their effect on peak noise; the noise model is then extended to multiple segmented aggressors by superposing the noise contributions of individual aggressors and sweeping the result in the time domain to determine the peak noise; estimating peak noise on the victim line for different configurations of aggressor victim overlaps; peak noise voltage on the victim net is calculated for the single Phi model first; then the segmented configuration is modeled using a three Phi model; the resulting analytical model and analytical expressions for noise and delay are excessively complicated

(**Kahng et al.,** "Noise model for multiple segmented coupled RC interconnects", IEEE 2001); and

(3) delay analysis of distributed RC line; determining common threshold crossing times of a finite length RC line with capacitive load termination; first order lumped Phi approximation to the finite length RC line terminated with a capacitive load is good enough for obtaining the 50% to 63.2% threshold crossing times of the step response; higher order lumped approximations are necessary for more accurate predictions of the 10% and 90% threshold crossing times; a second order Phi approximation to the distributed RC line is also used, where the RC line is split into two halves, each half approximated by a first order Phi approximation; the Phi-2 network is better than the Phi-1 network in determining the threshold crossing times (**Rao,** "Delay analysis of the distributed RC line", ACM 1995).

None of these references taken either alone or in combination with the prior art of record discloses a method for identifying potential noise failures in an integrated circuit design and an article of manufacture comprising one or more recordable medium having executable instructions stored thereon for identifying potential noise failures in an integrated circuit design, specifically including:

"modeling the victim net using two π-type resistor-capacitor (RC) circuits, wherein modeling the victim net using two π-type resistor-capacitor (RC) circuits comprises modeling the victim net with one π-type RC circuit before a coupling location and one π-type RC circuit after the coupling location; and determining a coupling between the victim net and the aggressor".

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

Paul L. Rodriguez 8/4/05
Primary Examiner
Art Unit 2125

K. Thangavelu
Art Unit 2123
July 29, 2005